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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,954	01/30/2004	Kenichi Tajika	61282-056	2504

EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

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DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,954	TAJIKA ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/30/04, 10/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it includes two paragraphs.

Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claim 2 is objected to because following informalities:

Applicant must clarify what is “a wiring length between the clock input terminal of the semiconductor chip and the area terminal is equal”. In other words it is readable as: “the length between point A and point B is equal???”

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 9, 11-12 and 15 are rejected under 35 U.S.C. 102(b) as being unpatentable by Erdal et al. (US Patent 5,686,845).

4. As to claims 1 and 6 Erdal discloses:

(1) A clock delay adjusting method of a semiconductor integrated circuit device,

wherein a plurality of source points for adjusting a clock delay is provided (buffers B, for example, - col.3, ll.42-46, Fig.4) in order to synchronize a value of the clock delay from each of the source points of each of hierarchical blocks in a semiconductor chip to a clock input circuit (clocked circuit elements or cells C in each block-Fig. 4) to be operated synchronously with a clock depending on a circuit design condition of the hierarchical block (means for minimizing the skew in the circuit and restore synchronism to the operation of the circuit. This function can be provided by inserting delay buffers in the circuit having different delays to compensate for the different values of delay at the individual blocks-col.1, ll.38-43) (col.1, ll.38-43; col.2, ll.49-67; col.3, ll.35-41);

an area terminal is provided in the source point (the source points for adjusting the clock delay are provided to be the area terminals - paragraph 21 of the Application) (delay buffer B will be provided typically at the first and second hierarchical block level-col.3, ll.52-53, Fig.4), and a clock input terminal of the semiconductor chip and each area terminal are connected through a clock line so as to be clock distributed over a hierarchical top (The clock pulses CLOCK are applied to a clock driver 64, which applies the clock pulses through an electrical interconnect wiring 66 to microelectronic

circuit modules or blocks 68, 70 and 72. The wiring 66 is connected to a clock delay buffer B in each block 68 and 70, and in each sub-block 72a, 72b and 72c. Although only two levels of hierarchy are illustrated in FIG. 4, consisting of one block level and one sub-block level, the invention is not so limited. A hierarchical structure including any number of block/sub-block levels can be provided in accordance with the present invention) (col.3, ll.42-53; col.3, ll.52-53); and

a clock delay between the hierarchical blocks is adjusted (Abstract; col.3, ll.55-57).

(6) A clock delay adjusting method of a semiconductor integrated circuit device, wherein an area terminal for a clock input is provided at least one place over at least one hierarchical block in a semiconductor chip in a clock wiring design of the semiconductor chip (the source points for adjusting the clock delay are provided to be the area terminals - paragraph 21 of the Application) (delay buffer B will be provided typically at the first and second hierarchical block level- col.3, ll.52-53, Fig.4), a clock input terminal of the semiconductor chip and the area terminal for a clock input are wired over a hierarchical top (The clock pulses CLOCK are applied to a clock driver 64, which applies the clock pulses through an electrical interconnect wiring 66 to microelectronic circuit modules or blocks 68, 70 and 72. The wiring 66 is connected to a clock delay buffer B in each block 68 and 70, and in each sub-block 72a, 72b and 72c. Although only two levels of hierarchy are illustrated in FIG. 4, consisting of one block level and one sub-block level, the invention is not so limited. A hierarchical structure including any number of block/sub-block levels can be provided in accordance

with the present invention); (col.3, ll.42-53; col.3, ll.52-53), a difference in a delay value between the area terminal and the clock input terminal is calculated (After the delay corresponding to each clocked cell C is determined, the value of delay which the buffer B is required to produce in order to equalize the delay at the inputs of all of the clocked cells C is calculated- col.5, ll.28-31), and a clock delay is adjusted from the area terminal 'to a plurality of clock input circuits in-order to compensate for the difference in the delay value in the hierarchical block (and one of the 20 possible buffer configurations is selected from the library set which has the corresponding value of delay. The buffers B are then inserted into the design and placed automatically in layout, based on the required delay values –col.5, ll.31-35) (col.3, ll.42-53; col.3, ll.52-53; col.3, ll.61-67; col.4, ll.24-31; col.5, ll.18-35).

5. As to claims 2-5, 9m 11-12 and 15 Erdal recites:

(2) The clock delay adjusting method, wherein at least one of the hierarchical blocks has a plurality of area terminals in such a manner that a wiring length between the clock input terminal of the semiconductor chip and the area terminal is equal (col.3, ll.55-60);

(3) The clock delay adjusting method, wherein the area terminal is a special input terminal for a clock input (col.4, ll.40-67; col.5, ll.1-18);

(4) The clock delay adjusting method, wherein the clock input terminal of the semiconductor chip and the area terminal are connected through a clock distribution (col.5, ll.19-36);

(5), (12) The clock delay adjusting method, wherein a delay adjusting buffer circuit is inserted (Abstract; col.3, ll.42-53; col.3, ll.52-57; col.3, ll.61-67; col.4, ll.24-31; col.5, ll.18-35);

(9) The clock delay adjusting method, wherein a number of the clock input circuits in the hierarchical block depends of delay value (col.3, ll.1-4; col.4, ll.40-67; col.5, ll.1-18; Fig. 5);

(11) The clock delay adjusting method, wherein the clock input terminal forms a multisystem clock (col.2, ll.49-59);

(15) A semiconductor integrated circuit device using the clock delay adjusting method semiconductor integrated circuit device (Abstract; col.1, ll.38-43; col.2, ll.49-67; col.3, ll.35-53; col.3, ll.55-57).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-8, 10, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erdal in view of Pileggi et al. (US Patent 6,651,232).

With respect to claims 7-8, 10, 14 and 16 Erdal teaches the features above but lacks a clock delay adjusting method of a semiconductor integrated circuit device, wherein a total the clock wiring length is almost the smallest, the clock line is formed by using a special layer and can be reused after floor plan correction.

As to claims 7-8, 10, 14 and 16 Pileggi teaches:

(7), (8) The clock delay adjusting method, wherein a total clock wiring length is almost the smallest (Abstract; col.3, ll.30-37);

(10), (16) The clock delay adjusting method, wherein the clock line is formed by using a special layer (col.3, ll.38-56);

(14) The clock delay adjusting method, wherein the clock line can be reused after floor plan correction (col.4, ll.64-67).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Pileggi's teaching regarding the clock delay adjusting method of a semiconductor integrated circuit device, wherein a total the clock wiring length is almost the smallest, the clock line is formed by using a special layer and can be reused after floor plan correction and use it Erdal's invention to provide clock tree/mesh construction concurrently with physical design, thereby increasing an efficiency of the integrated circuit design.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Erdal in view of Furuta et al. (US Patent 5,978,930).

With respect to claim 13 Erdal teaches the features above but lacks a clock delay adjusting method of a semiconductor integrated circuit device, wherein clock control circuit is inserted into the clock line.

As to claim 13 Furuta discloses:

a clock delay adjusting method of a semiconductor integrated circuit device, wherein clock control circuit is inserted into the clock line (Abstract; col.1, ll.60-67; col.2, ll.1-45; col.3, ll.51-67; col.4, ll.1-3).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Furuta's teaching regarding the clock delay adjusting method of a semiconductor integrated circuit device, wherein clock control circuit is inserted into the clock line and use it Erdal's invention to provide a clock signal control system having a clock stop signal generating circuit which is simple enough to miniaturize the system, reduce power consumption, and promote easy design, thereby increasing an efficiency of the integrated circuit design.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Alwando
THUAN DO
Primary examiner.
03/10/2006